REMARKS

Claims 1-19 and 26-33 are pending in the application. By the above amendment, claims 1, 3, 5, 9, 10, 11, 13, 15, 26, 27, 29, 32 and 33 have been amended, claims 2, 14, 28, 30 and 31 have been canceled without prejudice, and new claims 34~38 have been added. Applicants gratefully acknowledge Examiner's indication that claim 17 includes allowable subject matter. Reconsideration of the rejections and objections is respectfully requested in view of the following remarks.

Drawing Objections

FIGs. 8 and 9 of the drawings are objected to for not containing descriptive titles. Applicants believe that FIGs. 8 and 9 include descriptive title information and other graphical information which is clear with reference to the graphic illustrations and corresponding description in the specification. In this regard, withdrawal of the drawing objections is requested. In any event, Applicants are amenable to amending the Figures 8 and 9, but further clarification and specificity is required from the Examiner as to what should be added to these Figures.

Claim Rejections - 35 U.S.C. §102

Claims 1-3, 6-10, 12, 19, 26-29 and 32 stand rejected as being anticipated by $\underline{\text{Bastos}}$ et al. Applicants submit that at the very minimum, claims 1, 10, 26 and 27 are patentable distinguished and patentable over $\underline{\text{Bastos}}$. $\underline{\text{Bastos}}$ does not disclose or suggest, e.g., obtaining DC voltage characteristic data for a device pair having a first and second transistor, wherein the DC voltage characteristic data for a selected device pair comprises an output DC voltage V_{OUT} as a function of an input DC voltage V_{IN} , wherein V_{IN} is applied to a gate of at least one of the first and second transistors and wherein V_{OUT} is obtained at a common node connection of the first and second transistors, and

wherein the DC voltage characteristic data is obtained with the first and second transistor devices operating in a subthreshold region, as essentially claimed in claims 1, 10, 26 and 27.

In contrast, <u>Bastos</u> teaches a method for characterizing transistor mismatch by forming a test chip comprising a transistor array and then independently measuring the drain current of each transistor in the array sequentially with the transistor operating in saturation. (See page 271). Clearly, <u>Bastos</u> does <u>not</u> disclose or suggest obtaining *DC* voltage characteristic data as claimed.

For at least the above reasons, claims 1, 10, 26 and 27 (and all claims that depend there from) are distinguishable and not anticipated by <u>Bastos</u>. Accordingly, withdrawal of the anticipation rejections is requested.

Claim Rejections - 35 U.S.C. §103

The following obviousness rejections were asserted:

- (i) Claim 4 stands rejected as being unpatentable over <u>Bastos</u> in view of U.S. Patent No. 6,731,916 to <u>Haruyama</u>;
- (ii) Claims 5, 11, 30 and 31 stand rejected as being unpatentable over <u>Bastos</u> in view of <u>Conti</u>;
- (iii) Claims 13-16 and 33 stand rejected as being unpatentable over Bastos, Conti and U.S. Patent No. 4,851,768 to <u>Yoshizawa</u> et al; and
- (iv) Claim 18 stands rejected as being unpatentable over <u>Bastos</u> in view of U.S. Patent No. 6,181,621 to <u>Lovett</u>.

Each of the above obviousness rejections is based on the primary reference <u>Bastos</u> as applied to independent claims 1, 10 and 28. However, as noted above, <u>Bastos</u> does not

disclose or suggest various features of claims 1, 10 and 28. As such, the use of <u>Bastos</u> to establish a <u>prima facie</u> case of obviousness against the dependent claims of claims 1, 10 and 28 renders the obviousness rejections legally deficient on their face.

In any event, the cited references do not cure the deficiencies of <u>Bastos</u>. For instance, <u>Conti</u> is directed to a method for characterizing MOS transistor mismatch using output currents (see, e.g., page 137). <u>Lovett</u> is directed to a sense amplifier design that provides compensation for Vt mismatch, but does not remotely disclose or suggest a method for characterizing mismatch of device pairs. Further, <u>Haruyama</u> and <u>Yoshizawa</u> are simply irrelevant and not remotely related to the claimed inventions. Accordingly, withdrawal of the obviousness rejections is requested.

Respectfully submitted,

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